Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 2-27.

Listing of Claims:

1. (Original) A cache system comprising:

at least one DRAM array divided into a plurality of blocks;

first and second SRAM arrays each having a capacity at least as large as the capacity of a block of the DRAM array;

an address decoder coupled to receive a memory address and being operable to decode the address and generate decoded address signals corresponding thereto;

an input/output circuit coupled to the DRAM array, the SRAM array, and the address decoder, the input/output circuit being operable to respond to a first control signal by coupling write data from an external data terminal to a location in a block of the DRAM array corresponding to the decoded address signals, or to respond to a second control signal by coupling write data from the external data terminal to a location in the first or second SRAM arrays, or to respond to a third control signal by coupling data from one of the SRAM arrays to a location in a block of the DRAM array corresponding to the decoded address signals; and

a control circuit coupled to the DRAM array, the SRAM array, the address decoder, and the input/output circuit, the control circuit being operable to refresh the DRAM array one block at a time, the control circuit further being operable to generate the first control signal when the block of the DRAM array corresponding to the decoded address signals is not being refreshed, to generate the second control signal when the block of the DRAM array corresponding to the decoded address signals is being refreshed, to generate the third control signal when the block of the DRAM array that was being refreshed when the data was stored in the SRAM array is no longer being refreshed.

Claims 2-27 (Cancelled)